Response To Office Action Mailed February 27, 2003

A. Pending Claims

Claims 28-32 are currently pending. Claims 28, 29, 31, and 32 have been amended. Support for the amendment to claim 28 may be found in the Specification at least on page 4, lines 7-14. Claims 29, 31, and 32 have been amended for clarification and/or correction of typographical errors. Claims 18-27 and 33-55 have been canceled.

B. Election/Restrictions

The Examiner states: "Newly submitted claims 37-55 are directed to an invention that is independent or distinct from the invention originally claimed....Since applicant has received an action on the merits for the originally presented invention, this invention has been constructively elected by original presentation for prosecution on the merits."

Applicant hereby elects the invention of claims 18-36, drawn to a method of making a semiconductor device, class 438, without traverse. Applicant reserves the right to file divisional applications capturing the subject matter of the non-elected invention. Applicant believes that all presently pending claims are directed to the elected subject matter.

C. The Claims Are Not Obvious Over Chittipeddi In View of Bergeron Pursuant To 35 U.S.C. 103(a)

The Examiner rejected claims 28-30, 33, and 34 under 35 U.S.C. 103(a) as obvious over U.S. Patent No. 5,918,116 to Chittipeddi (hereinafter "Chittipeddi") in view of U.S. Patent No. 4,157,268 to Bergeron et al. (hereinafter "Bergeron"). Applicant respectfully disagrees with these rejections.

In order to reject a claim as obvious, the Examiner has the burden of establishing a *prima*

facie case of obviousness. *In re Warner et al.*, 379 F.2d 1011, 154 U.S.P.Q. 173, 177-178 (C.C.P.A. 1967). To establish a *prima facie* obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. *In re Royka*, 490 F.2d 981, 180 U.S.P.Q. 580 (C.C.P.A. 1974), MPEP § 2143.03.

The Examiner states:

> Regarding claims 23-25, 28-30, 33 and 34, Chittipeddi discloses implanting predetermined regions of a silicon substrate (10) with a dose of 1 x 10^{12} to about 5 x 10^{16} ions/cm^2 ions (18) at an implantation energy of 5-500 keV with an implanted dose of (Fig. 5; col. 2, ln. 48-54; col. 3, ln. 19-37). The surface of the silicon substrate is oxidized to form a gate oxide layer (22) of non-uniform thickness and MOS transistors are formed at the predetermined regions of the substrate such that the oxidized layer at the predetermined regions forms the gate oxide layer of the MOS transistors (Fig. 7; col. 3, ln. 66-col. 4, ln. 26;col. 3, ln. 45-58). Chittipeddi discloses that the ions (18) are "selected for their ability to amorphize the epitaxial silicon layer 10 [substrate]" and, "[S]uch ions include silicon, fluorine, arsenic, and mixtures thereof" (col. 3, ln. ... Like Chittipeddi, Bergeron discloses a method of implanting ions (18) into a silicon substrate (10) in order to damage the crystalline structure of the substrate an dthen subjecting the substrate to an oxidation process in order to oxidize the damaged substrate regions (col. 3, ln. 39-50). Bergeron discloses that the ions used to damage/amorphize the substrate may be silicon, helium, neon or argon (col. 3, ln. 42-43). At the time of the invention, it would have been obvious to one of ordinary skill in the art to substitute any one of helium, neon or argon ions for the silicon ions disclosed by Chittipeddi as a matter of design choice because Chittipeddi discloses that ions are chosen only for their ability to amorphize the silicon substrate and Bergeron teaches that any of these ions (He, Ne, Ar or Si) may be used for that purpose.

Amended claim 28 describes a combination of features including:

> implanting a chemical species, with an implantation energy between 2 and 15 keV, into the predetermined regions of the silicon substrate, wherein the chemical species comprises Ar, Ne or He, and wherein the predetermined regions of the silicon substrate are exposed directly to the implantation source; oxidizing the surface of the silicon substrate to form a gate oxide layer of non-uniform thickness; and forming MOS transistors at the predetermined regions of the silicon substrate, wherein the oxidized layer at the predetermined regions forms the gate oxide layer of the MOS transistors.

Chittipeddi appears to teach requiring a first oxide layer to be formed on an epitaxial silicon layer to prevent excess damage to the epitaxial silicon layer during ion implantation and to help adjust the dosage and/or energy of the implant. Chittipeddi also appears to teach removing the first oxide layer before forming the gate oxide layer. For example, Chittipeddi states:

> Oxide layer 12 is then preferably grown on epitaxial silicon layer 10 as illustrated in FIG. 3. (Chittipeddi, column 3, lines 3-4)
>
> Turning now to FIG. 5, ions 18 are implanted by implantation means (not shown) such that ions 18 pass through window 16 and penetrate the exposed area of oxide layer 12 and epitaxial silicon layer 10 underlying the exposed area of oxide layer 12. Implantation of ions 18 in epitaxial silicon layer 10 damages, i.e., amorphizes, the crystal lattice structure of epitaxial silicon layer 10. FIG. 6 depicts amorphized region 20 where ions 18 are implanted in a selected region of epitaxial silicon layer 10. Oxide layer 12 partly serves the function of preventing excess damage to epitaxial silicon layer 10 from occurring when ions 18 are implanted in epitaxial silicon layer 10. (Chittipeddi, column 3, lines 19-30)
>
> The dosage and/or energy of such an amorphizing implant will vary depending upon the thickness of exposed oxide layer 12 and the amount of damage to epitaxial silicon layer 10 which is desired. (Chittipeddi, column 3, lines 42-45)
>
> Following such an annealing step, oxide layer 12 is removed by any suitable method, e.g., chemical etching, utilizing known and conventional techniques, e.g., a 10:1 HF solution.
>
> Gate oxide 22 is subsequently grown on epitaxial silicon layer 10 as shown in FIG. 1. Gate oxide 22 can be grown on epitaxial silicon layer 10 by any suitable growth technique. (Chittipeddi, column 3, line 61 – column 4, line 1)

Chittipeddi does not appear to teach or suggest exposing a silicon substrate without an overlying layer directly to an ion implantation source.

The invention of Bergeron relates to a process for making bipolar transistors. Bergeron

appears to teach damaging an epitaxial region to enhance the rate of oxidation in one step of the process in order to form a thinned epitaxial layer in which base and collector structures can be formed. For example, Bergeron states:

> By reducing the epitaxial layer thickness for the upward injecting vertical transistors in the I^2L circuits, the charge storage characteristic of the device is reduced and the injection efficiency of the device is increased. By increasing the epitaxial thickness in the downward injecting vertical transistors used for the off chip drivers and receivers, a larger signal voltage can be employed since the base to subcollector junction has a higher breakdown voltage characteristic. A method is disclosed for forming this structure which employs the technique of introducing damage in the epitaxial region above the buried subemitter of the I^2L vertical transistor so as to enhance the reactivity of the epitaxial surface to a subsequent oxidation reaction step. By increasing the rate of oxidation in the epitaxial layer, a locally thinned region can be formed, into which the base and collector structures can be subsequently formed using the same steps as are employed to form the base and emitter structures in the downward injection NPN used as the off chip driver device. (Bergeron, column 1, line 57 – column 2, line 9)

Bergeron does not appear to teach or suggest enhancing an oxidation reaction step in a process for forming a gate oxide layer in a MOS transistor. Applicant submits that Chittipeddi in forming a MOS-type device would have had no motivation to use the chemical species taught in the process for forming a bipolar transistor of Bergeron. Furthermore, Bergeron teaches the implantation of chemical species without the use of an overlying layer. Chittipeddi, however, teaches the importance of retaining an overlying layer to protect the underlying silicon substrate from excess damage. Applicant submits that it would not be obvious to use the chemical species of Bergeron in Chittipeddi without the use of a barrier layer to reduce damage, as Chittipeddi teaches the importance of minimizing the damage to the silicon substrate.

Obviousness can only be established by "showing some objective teaching in the prior art or that knowledge generally available to one of ordinary skill in the art would lead that individual to combine the relevant teaching of the references." *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988).

Applicant's claim is directed to a combination of features including the features of "implanting a chemical species, with an implantation energy between 2 and 15 keV, into the predetermined regions of the silicon substrate, wherein the chemical species comprises Ar, Ne or He, and wherein the predetermined regions of the silicon substrate comprise no overlying layer and are exposed directly to the implantation source". Applicant submits that at least these features, in combination with the other features of the claim, are not taught or suggested by Chittipeddi in view of Bergeron. If an independent claim is nonobvious under 35 U.S.C. 103, then any claim depending therefrom is nonobvious. *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988). Applicant respectfully requests removal of the rejection of claim 28 and the claims dependent thereon.

D. The Claims Are Not Obvious Over Chittipeddi In View of Bergeron and Further In View of Tzeng Pursuant To 35 U.S.C. 103(a)

The Examiner rejected claims 31 and 32 under 35 U.S.C. 103(a) as obvious over Chittipeddi in view of Bergeron and further in view of U.S. Patent No. 5,215,934 to Tzeng (hereinafter "Tzeng"). Applicant respectfully disagrees with these rejections.

The Examiner states: "Regarding claims 26, 27, 31, 32, 35 and 36, Chittipeddi discloses that the gate oxide layer can be grown by "any suitable technique", which may include heating the substrate to a temperature of 600-1200°C and subjecting the substrate to a wet or dry O2 atmosphere (col. 3, ln. 67-col. 4, ln. 6)....Like Chittipeddi, Tzeng discloses a method of thermally oxidizing a silicon substrate that has been implanted with oxidation-rate-enhancing ions (Abstract)."

Amended claim 31 describes a combination of features including:

> wherein oxidizing the surface of the silicon substrate comprises oxidation in a furnace, plasma oxidation, electrochemical oxidation or rapid thermal oxidation.

Chittipeddi appears to teach or suggest oxidation at temperatures from 600 to 1200 °C with wet or dry O_2. For example, Chittipeddi states:

> Typically, gate oxide layer 22 is grown on epitaxial silicon layer 10 by heating the substrate to a temperature ranging from about 600 to about 1200° C., Preferably from about 700 to about 900° C., and subjecting the substrate to oxidation, such as wet or dry O_2. (Chittipeddi, column 4, lines 2-6)

Tzeng appears to teach or suggest oxidation in a furnace. For example, Tzeng states:

> The thermal oxidation takes place in a furnace at a temperature of around 950° C. for a period of approximately 10 minutes in a dry O_2 atmosphere. (Tzeng, column 6, lines 11-14)

Neither Chittipeddi nor Tzeng appear to teach oxidation by plasma oxidation, electrochemical oxidation or rapid thermal oxidation. Applicant's claim is directed to a combination of features including the features "wherein oxidizing the surface of the silicon substrate comprises oxidation in a furnace, plasma oxidation, electrochemical oxidation or rapid thermal oxidation." Applicant submits that at least these features, in combination with the other features of the independent claim, are not taught or suggested by Chittipeddi in view of Bergeron and further in view of Tzeng. Applicant respectfully requests removal of the rejection of claim 31.

E. Summary

Based on the above, Applicant submits that all claims are now in condition for allowance. Favorable reconsideration is respectfully requested.

Applicant believes that no fees are due in association with the filing of this document. If any extension of time is required, Applicant hereby requests the appropriate extension of time. If any fees are required, please charge those fees to Meyertons, Hood, Kivlin, Kowert & Goetzel, P.C. Deposit Account Number 50-1505/5310-03000/EBM.

Respectfully submitted,

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